ESP32-S3-PICO-1 Series

Datasheet

2.4 GHz Wi-Fi + Bluetooth® LE SiP
Supporting IEEE 802.11b/g/n (2.4 GHz Wi-Fi) and Bluetooth® 5 (LE)
Integrating all peripheral components in one single package

Including:

ESP32-S3-PICO-1-N8R2

ESP32-S3-PICO-1-N8R8

Version 1.0
Espressif Systems

Product Overview

ESP32-S3-PICO-1 is a System-in-Package (SiP) device that is based on ESP32-S3 with integrated 2.4 GHz Wi-Fi and Bluetooth® Low Energy (Bluetooth LE). It integrates an 8 MB SPI flash and an up to 8 MB SPI PSRAM.

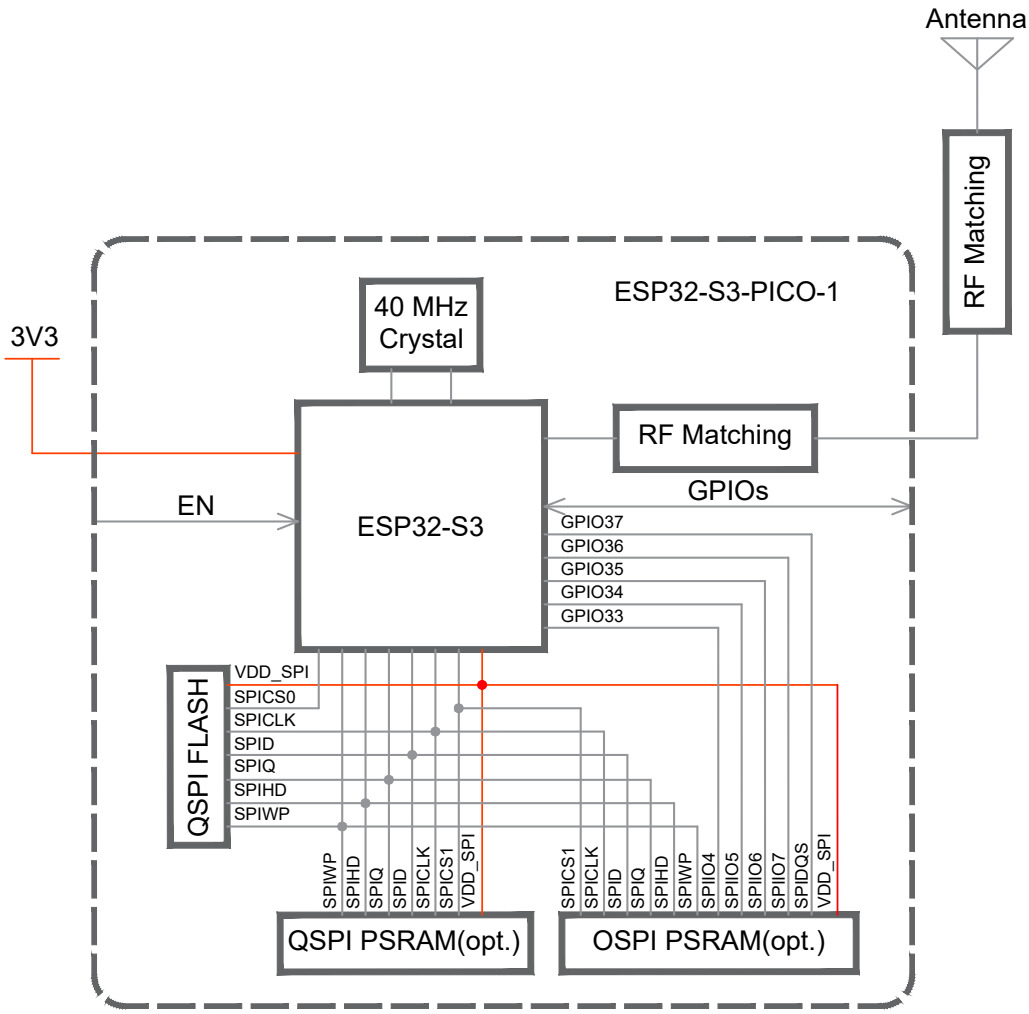
ESP32-S3-PICO-1 provides complete Wi-Fi and Bluetooth® functionalities and is designed with the TSMC low-power 40 nm technology. It seamlessly integrates all peripheral components, including a crystal oscillator, decoupling capacitors, SPI flash/PSRAM, and RF matching links, within a single package. As a result, there is no need for additional peripheral components, simplifying the soldering and testing processes. It also streamlines the supply chain and enhances control and management efficiency.

With its ultra-small size, robust performance, and low-energy consumption, ESP32-S3-PICO-1 is well suited for any space-limited or battery-operated applications, such as wearable electronics, medical equipment, sensors and other IoT products.

At the core of ESP32-S3-PICO-1 is the ESP32-S3 chip, a low-power MCU-based system on a chip (SoC) with integrated 2.4 GHz Wi-Fi and Bluetooth® Low Energy (Bluetooth LE). It consists of high-performance dual-core microprocessor (Xtensa® 32-bit LX7), a low-power coprocessor, a Wi-Fi baseband, a Bluetooth LE baseband, RF module, and numerous peripherals. For more details on ESP32-S3, please refer to *ESP32-S3 Series Datasheet*.

Block Diagram

The block diagram of ESP32-S3-PICO-1 is shown below.



ESP32-S3-PICO-1 Block Diagram

Features

CPU and Memory

- ESP32-S3 SoC embedded, Xtensa® dual-core 32-bit LX7 microprocessor (with single precision FPU), up to 240 MHz
- 384 KB ROM
- 512 KB SRAM
- 16 KB SRAM in RTC

Wi-Fi

- 802.11b/g/n
- Bit rate: 802.11n up to 150 Mbps
- TX/RX A-MPDU, TX/RX A-MSDU
- 0.4 μs guard interval support
- Center frequency range of operating channel: 2412 ~ 2484 MHz

Bluetooth

- Bluetooth LE: Bluetooth 5, Bluetooth mesh
- Speed: 125 Kbps, 500 Kbps, 1 Mbps, 2 Mbps
- Advertising extensions
- Multiple advertisement sets

- Channel selection algorithm #2
- Internal co-existence mechanism between Wi-Fi and Bluetooth to share the same antenna

Peripherals

- GPIO, SPI, LCD interface, Camera interface, UART, I2C, I2S, remote control, pulse counter, LED PWM, USB 1.1 OTG, USB Serial/JTAG controller, MCPWM, SD/MMC host, GDMA, TWAI® controller (compatible with ISO 11898-1), ADC, touch sensor, temperature sensor, timers and watchdogs

> **Note:**
> * Please refer to *ESP32-S3 Series Datasheet* for detailed information about the peripherals.

Integrated Components

- 40 MHz crystal oscillator
- 8 MB Quad SPI flash
- Up to 8 MB PSRAM

Operating Conditions

- Operating voltage/Power supply: 3.0 ~ 3.6 V
- Operating ambient temperature:
  - ESP32-S3-PICO-1-N8R2: –40 ~ 85 °C
  - ESP32-S3-PICO-1-N8R8: –40 ~ 65 °C

Applications (A Nonexhaustive List)

- Generic Low-power IoT Sensor Hub
- Generic Low-power IoT Data Loggers
- Cameras for Video Streaming
- Over-the-top (OTT) Devices
- USB Devices
- Speech Recognition
- Image Recognition
- Mesh Network
- Home Automation
- Smart Building
- Industrial Automation
- Smart Agriculture
- Audio Applications
- Health Care Applications
- Wi-Fi-enabled Toys
- Wearable Electronics
- Retail & Catering Applications

Note:

Check the link or the QR code to make sure that you use the latest version of this document:
https://www.espressif.com/documentation/esp32-s3-pico-1_datasheet_en.pdf

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1.1 ESP32-S3-PICO-1 Series Nomenclature

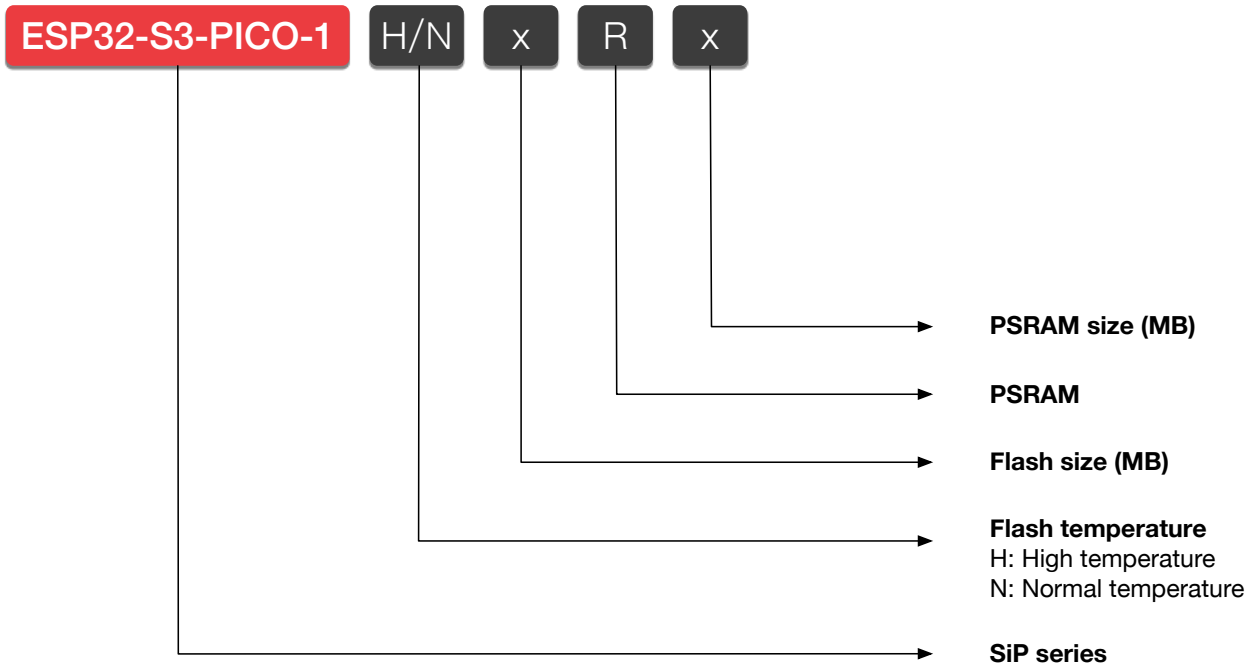


Figure 1-1. ESP32-S3-PICO-1 Series Nomenclature

1.2 Comparison

Table 1-1. ESP32-S3-PICO-1 Series Comparison

Ordering Code[1]	In-Package flash	In-Package PSRAM	Ambient Temp.[2] (°C)	SPI Voltage
ESP32-S3-PICO-1-N8R2	8 MB (Quad SPI)	2 MB (Quad SPI)	–40 ~ 85	3.3 V
ESP32-S3-PICO-1-N8R8[3]	8 MB (Quad SPI)	8 MB (Octal SPI)	–40 ~ 65	3.3 V

[1] For details on chip marking and packing, see Section 6 Packaging.

[2] Ambient temperature specifies the recommended temperature range of the environment immediately outside an Espressif chip.

[3] The ESP32-S3-PICO-1-N8R8 is still in sample status.

2 Pin Definition

2.1 Pin Layout

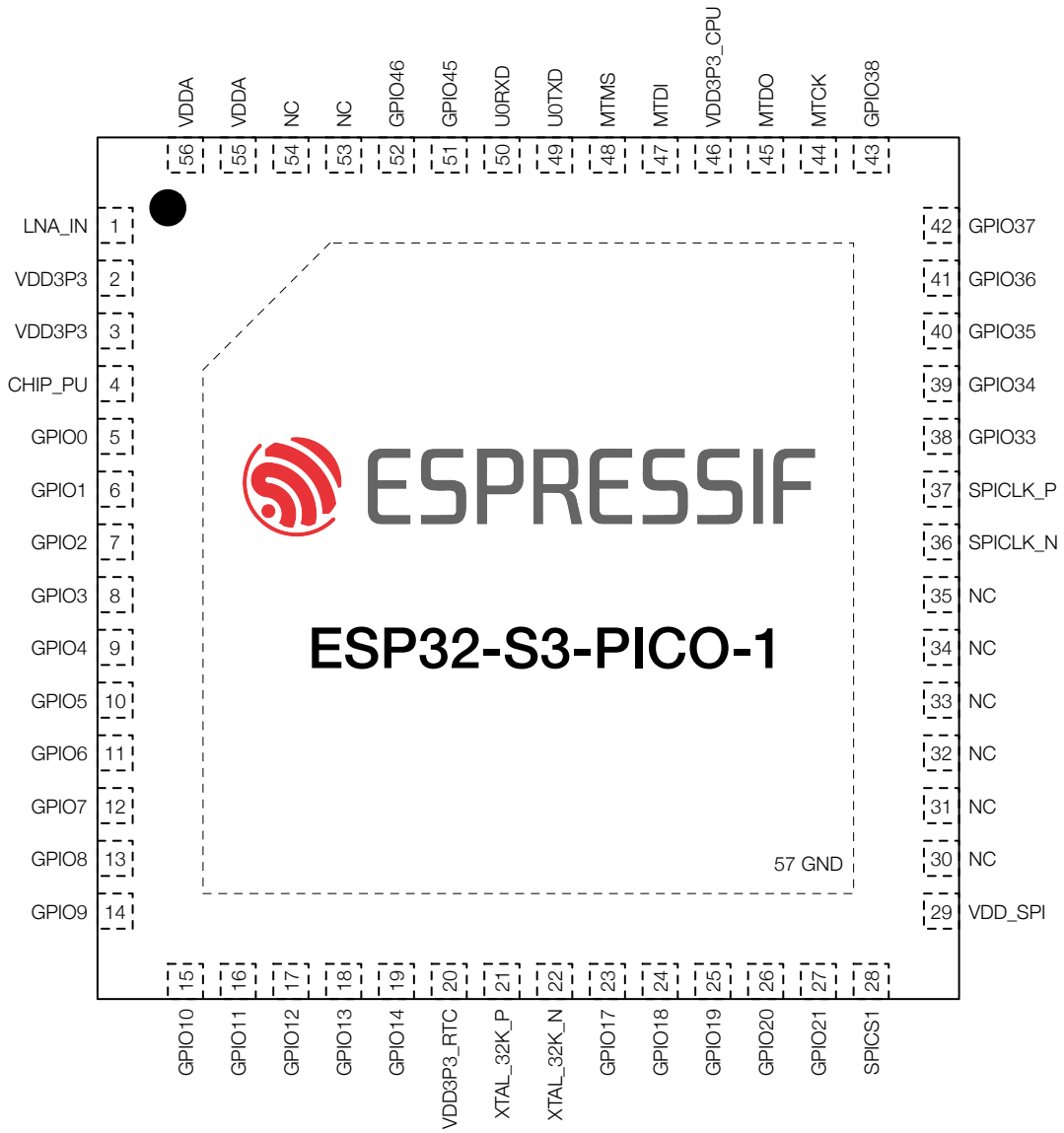


Figure 2-1. ESP32-S3-PICO-1 Pin Layout (Top View)

2.2 Pin Description

Table 2-1. Pin Description

Name	No.	Type[1]	Power Domain	Function[2, 5]
LNA_IN	1	I/O	—	Low Noise Amplifier (RF LNA) input and output signal
VDD3P3	2	P_A	—	Analog power supply
VDD3P3	3	P_A	—	Analog power supply
CHIP_PU	4	I	VDD3P3_RTC	High: on, enables ESP32-S3-PICO-1. Low: off, ESP32-S3-PICO-1 powers off. Note: Do not leave the CHIP_PU pin floating.
GPIO0	5	I/O/T	VDD3P3_RTC	RTC_GPIO0, **GPIO0**
GPIO1	6	I/O/T	VDD3P3_RTC	RTC_GPIO1, **GPIO1**, TOUCH1, ADC1_CH0
GPIO2	7	I/O/T	VDD3P3_RTC	RTC_GPIO2, **GPIO2**, TOUCH2, ADC1_CH1
GPIO3	8	I/O/T	VDD3P3_RTC	RTC_GPIO3, **GPIO3**, TOUCH3, ADC1_CH2
GPIO4	9	I/O/T	VDD3P3_RTC	RTC_GPIO4, **GPIO4**, TOUCH4, ADC1_CH3
GPIO5	10	I/O/T	VDD3P3_RTC	RTC_GPIO5, **GPIO5**, TOUCH5, ADC1_CH4
GPIO6	11	I/O/T	VDD3P3_RTC	RTC_GPIO6, **GPIO6**, TOUCH6, ADC1_CH5
GPIO7	12	I/O/T	VDD3P3_RTC	RTC_GPIO7, **GPIO7**, TOUCH7, ADC1_CH6
GPIO8	13	I/O/T	VDD3P3_RTC	RTC_GPIO8, **GPIO8**, TOUCH8, ADC1_CH7, SUBSPICS1
GPIO9	14	I/O/T	VDD3P3_RTC	RTC_GPIO9, **GPIO9**, TOUCH9, ADC1_CH8, SUBSPIHD, FSPIHD
GPIO10	15	I/O/T	VDD3P3_RTC	RTC_GPIO10, **GPIO10**, TOUCH10, ADC1_CH9, FSPIIO4, SUBSPICS0, FSPICS0
GPIO11	16	I/O/T	VDD3P3_RTC	RTC_GPIO11, **GPIO11**, TOUCH11, ADC2_CH0, FSPIIO5, SUBSPID, FSPID
GPIO12	17	I/O/T	VDD3P3_RTC	RTC_GPIO12, **GPIO12**, TOUCH12, ADC2_CH1, FSPIIO6, SUBSPICLK, FSPICLK
GPIO13	18	I/O/T	VDD3P3_RTC	RTC_GPIO13, **GPIO13**, TOUCH13, ADC2_CH2, FSPIIO7, SUBSPIQ, FSPIQ
GPIO14	19	I/O/T	VDD3P3_RTC	RTC_GPIO14, **GPIO14**, TOUCH14, ADC2_CH3, FSPIDQS, SUBSPIWP, FSPIWP
VDD3P3_RTC	20	P_A	—	Analog power supply
XTAL_32K_P	21	I/O/T	VDD3P3_RTC	RTC_GPIO15, **GPIO15**, U0RTS, ADC2_CH4, XTAL_32K_P
XTAL_32K_N	22	I/O/T	VDD3P3_RTC	RTC_GPIO16, **GPIO16**, U0CTS, ADC2_CH5, XTAL_32K_N
GPIO17	23	I/O/T	VDD3P3_RTC	RTC_GPIO17, **GPIO17**, U1TXD, ADC2_CH6

Name	No.	Type[1]	Power Domain	Function[2, 5]
GPIO18	24	I/O/T	VDD3P3_RTC	RTC_GPIO18, **GPIO18**, U1RXD, ADC2_CH7, CLK_OUT3
GPIO19	25	I/O/T	VDD3P3_RTC	RTC_GPIO19, GPIO19, U1RTS, ADC2_CH8, CLK_OUT2, **USB_D-**
GPIO20	26	I/O/T	VDD3P3_RTC	RTC_GPIO20, GPIO20, U1CTS, ADC2_CH9, CLK_OUT1, **USB_D+**
GPIO21	27	I/O/T	VDD3P3_RTC	RTC_GPIO21, **GPIO21**
SPICS1[4]	28	I/O/T	VDD_SPI	SPICS1, **GPIO26**
VDD_SPI	29	P_D	—	Output power supply: VDD3P3_RTC
NC	30	—	—	NC
NC	31	—	—	NC
NC	32	—	—	NC
NC	33	—	—	NC
NC	34	—	—	NC
NC	35	—	—	NC
SPICLK_N[3]	36	I/O/T	VDD3P3_CPU / VDD_SPI	SPICLK_N_DIFF, **GPIO48**, SUBSPICLK_N_DIFF
SPICLK_P[3]	37	I/O/T	VDD3P3_CPU / VDD_SPI	SPICLK_P_DIFF, **GPIO47**, SUBSPICLK_P_DIFF
GPIO33[3, 4]	38	I/O/T	VDD3P3_CPU / VDD_SPI	SPIIO4, **GPIO33**, FSPIHD, SUBSPIHD
GPIO34[3, 4]	39	I/O/T	VDD3P3_CPU / VDD_SPI	SPIIO5, **GPIO34**, FSPICS0, SUBSPICS0
GPIO35[3, 4]	40	I/O/T	VDD3P3_CPU / VDD_SPI	SPIIO6, **GPIO35**, FSPID, SUBSPID
GPIO36[3, 4]	41	I/O/T	VDD3P3_CPU / VDD_SPI	SPIIO7, **GPIO36**, FSPICLK, SUBSPICLK
GPIO37[3, 4]	42	I/O/T	VDD3P3_CPU / VDD_SPI	SPIDQS, **GPIO37**, FSPIQ, SUBSPIQ
GPIO38	43	I/O/T	VDD3P3_CPU	**GPIO38**, FSPIWP, SUBSPIWP
MTCK	44	I/O/T	VDD3P3_CPU	**MTCK**, GPIO39, CLK_OUT3, SUBSPICS1
MTDO	45	I/O/T	VDD3P3_CPU	**MTDO**, GPIO40, CLK_OUT2
VDD3P3_CPU	46	P_D	—	Input power supply for CPU IO
MTDI	47	I/O/T	VDD3P3_CPU	**MTDI**, GPIO41, CLK_OUT1
MTMS	48	I/O/T	VDD3P3_CPU	**MTMS**, GPIO42
U0TXD	49	I/O/T	VDD3P3_CPU	**U0TXD**, GPIO43, CLK_OUT1
U0RXD	50	I/O/T	VDD3P3_CPU	**U0RXD**, GPIO44, CLK_OUT2
GPIO45	51	I/O/T	VDD3P3_CPU	**GPIO45**
GPIO46	52	I/O/T	VDD3P3_CPU	**GPIO46**

Name	No.	Type[1]	Power Domain	Function[2, 5]
NC	53	—	—	NC
NC	54	—	—	NC
VDDA	55	P_A	—	Analog power supply
VDDA	56	P_A	—	Analog power supply
GND	57	G	—	Ground

[1] P: power pin; P_A: analog power pin; P_D: digital power pin; I: input; O: output; T: high impedance; NC: no component.

[2] Pin functions in bold font are the default pin functions in SPI Boot mode. For pins No.38 ∼ 42, the default function is decided by eFuse bit.

[3] Power supply for GPIO33 ∼ GPIO37, GPIO47 and GPIO48 is configurable to be either VDD3P3_CPU (default) or VDD_SPI.

[4] For ESP32-S3-PICO-1-N8R2, SPICS1 is connected to the Quad SPI PSRAM and is not available for other uses. For ESP32-S3-PICO-1-N8R8, SPICS1 and GPIO33 ∼ GPIO37 are connected to the Octal SPI PSRAM and are not available for other uses.

[5] The pin function in this table refers only to some fixed settings and do not cover all cases for signals that can be input and output through the GPIO matrix. For more information on the GPIO matrix, please refer to *ESP32-S3 Technical Reference Manual*.

2.3 Strapping Pins

At each startup or reset, the ESP32-S3-PICO-1 requires some initial configuration parameters, such as in which boot mode to load the SiP, voltage of flash memory, etc. These parameters are passed over via the strapping pins. After reset, the strapping pins operate as regular IO pins.

The parameters controlled by the given strapping pins at SiP reset are as follows:

- **Chip boot mode** – GPIO0 and GPIO46
- **VDD_SPI voltage** – GPIO45
- **ROM messages printing** – GPIO46
- **JTAG signal source** – GPIO3

GPIO0, GPIO45, and GPIO46 are connected to the chip's internal weak pull-up/pull-down resistors at chip reset. These resistors determine the default bit values of the strapping pins. Also, these resistors determine the bit values if the strapping pins are connected to an external high-impedance circuit.

Table 2-2. Default Configuration of Strapping Pins

Strapping Pin	Default Configuration	Bit Value
GPIO0	Pull-up	1
GPIO3	Floating	–
GPIO45	Pull-down	0
GPIO46	Pull-down	0

To change the bit values, the strapping pins should be connected to external pull-down/pull-up resistances. If the ESP32-S3-PICO-1 is used as a device by a host MCU, the strapping pin voltage levels can also be controlled by the host MCU.

All strapping pins have latches. At system reset, the latches sample the bit values of their respective strapping pins and store them until the chip is powered down or shut down. The states of latches cannot be changed in any other way. It makes the strapping pin values available during the entire chip operation, and the pins are freed up to be used as regular IO pins after reset.

Regarding the timing requirements for the strapping pins, there are such parameters as *setup time* and *hold time*. For more information, see Table 2-3 and Figure 2-2.

Table 2-3. Description of Timing Parameters for the Strapping Pins

Parameter	Description	Min (ms)
t_{SU}	*Setup time* is the time reserved for the power rails to stabilize before the CHIP_PU pin is pulled high to activate the chip.	0
t_{H}	*Hold time* is the time reserved for the chip to read the strapping pin values after CHIP_PU is already high and before these pins start operating as regular IO pins.	3

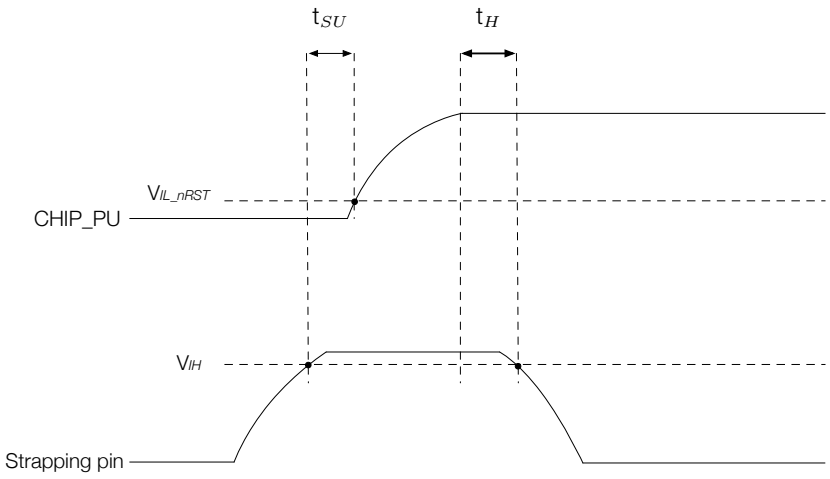


Figure 2-2. Visualization of Timing Parameters for the Strapping Pins

2.3.1 Chip Boot Mode Control

GPIO0 and GPIO46 control the boot mode after the reset is released. See Table 2-4 Chip Boot Mode Control.

Table 2-4. Chip Boot Mode Control

Boot Mode	GPIO0	GPIO46
Default Configuration	1 (Pull-up)	0 (Pull-down)
SPI Boot (default)	1	Any value
Download Boot	0	0
Invalid combination [1]	0	1

[1] This combination triggers unexpected behavior and should be avoided.

2.3.2 VDD_SPI Voltage Control

The required VDD_SPI voltage for ESP32-S3-PICO-1 can be found in Table 1-1 Comparison.

Depending on the value of EFUSE_VDD_SPI_FORCE, the voltage can be controlled in two ways.

Table 2-5. VDD_SPI Voltage Control

EFUSE_VDD_SPI_FORCE	GPIO45	eFuse [1]	Voltage	VDD_SPI power source [2]
0	0	Ignored	3.3 V	VDD3P3_RTC via R_{SPI}
	1		1.8 V	Flash Voltage Regulator
1	Ignored	0	1.8 V	Flash Voltage Regulator
		1	3.3 V	VDD3P3_RTC via R_{SPI}

[1] eFuse: EFUSE_VDD_SPI_TIEH

[2] See *ESP32-S3 Series Datasheet* > Section *Power Scheme*

2.3.3 ROM Messages Printing Control

During boot process the messages by the ROM code can be printed to:

- (Default) UART and USB Serial/JTAG controller.
- USB Serial/JTAG controller.
- UART.

The ROM messages printing to UART or USB Serial/JTAG controller can be respectively disabled by configuring registers and eFuse. For detailed information, please refer to *ESP32-S3 Technical Reference Manual* > Chapter *Chip Boot Control*.

2.3.4 JTAG Signal Source Control

The strapping pin GPIO3 can be used to control the source of JTAG signals during the early boot process. This pin does not have any internal pull resistors and the strapping value must be controlled by the external circuit that cannot be in a high impedance state.

As Table 2-6 shows, GPIO3 is used in combination with EFUSE_DIS_PAD_JTAG, EFUSE_DIS_USB_JTAG, and EFUSE_STRAP_JTAG_SEL.

Table 2-6. JTAG Signal Source Control

eFuse 1[a]	eFuse 2[b]	eFuse 3[c]	GPIO3	JTAG Signal Source
0	0	0	Ignored	USB Serial/JTAG Controller
		1	0	JTAG pins MTDI, MTCK, MTMS, and MTDO
			1	USB Serial/JTAG Controller
0	1	Ignored	Ignored	JTAG pins MTDI, MTCK, MTMS, and MTDO
1	0	Ignored	Ignored	USB Serial/JTAG Controller
1	1	Ignored	Ignored	JTAG is disabled

[a] eFuse 1: EFUSE_DIS_PAD_JTAG
[b] eFuse 2: EFUSE_DIS_USB_JTAG
[c] eFuse 3: EFUSE_STRAP_JTAG_SEL

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Stresses above those listed in Table 3-1 *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and normal operation of the device at these or any other conditions beyond those indicated in Section 3.2 Recommended Power Supply Characteristics is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 3-1. Absolute Maximum Ratings

Parameter	Description	Min	Max	Unit
VDDA, VDD3P3, VDD3P3_RTC, VDD3P3_CPU, VDD_SPI	Allowed input voltage	–0.3	3.6	V
I_{output} [1]	Cumulative IO output current	—	1500	mA
T_{STORE}	Storage temperature	–40	150	°C

[1] The product proved to be fully functional after all its IO pins were pulled high while being connected to ground for 24 consecutive hours at ambient temperature of 25 °C.

3.2 Recommended Power Supply Characteristics

For recommended ambient temperature, see Section 1 ESP32-S3-PICO-1 Series Comparison.

Table 3-2. Recommended Power Characteristics

Parameter [1]	Description	Min	Typ	Max	Unit
VDDA, VDD3P3	Recommended input voltage	3.0	3.3	3.6	V
VDD3P3_RTC [2]	Recommended input voltage	3.0	3.3	3.6	V
VDD_SPI (as input)	—	1.8	3.3	3.6	V
VDD3P3_CPU [3]	Recommended input voltage	3.0	3.3	3.6	V
I_{VDD} [4]	Cumulative input current	0.5	—	—	A

[1] If VDD3P3_RTC is used to power VDD_SPI, the voltage drop on R_{SPI} should be accounted for. See also Section 3.3 VDD_SPI Output Characteristics.

[2] If writing to eFuses, the voltage on VDD3P3_CPU should not exceed 3.3 V as the circuits responsible for burning eFuses are sensitive to higher voltages.

[3] If you use a single power supply, the recommended output current is 500 mA or more.

3.3 VDD_SPI Output Characteristics

Table 3-3. VDD_SPI Internal and Output Characteristics

Parameter	Description [1]	Typ	Unit
R_{SPI}	VDD_SPI powered by VDD3P3_RTC via R_{SPI} for 3.3 V flash/PSRAM [2]	14	Ω

[1] VDD3P3_RTC must be more than *VDD_flash_min* + *I_flash_max* * R_{SPI}; where

- *VDD_flash_min* – minimum operating voltage of flash/PSRAM
- *I_flash_max* – maximum operating current of flash/PSRAM

3.4 DC Characteristics (3.3 V, 25 °C)

Table 3-4. DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN}	Pin capacitance	—	2	—	pF
V_{IH}	High-level input voltage	0.75 × VDD[1]	—	VDD[1]+ 0.3	V
V_{IL}	Low-level input voltage	–0.3	—	0.25 × VDD[1]	V
I_{IH}	High-level input current	—	—	50	nA
I_{IL}	Low-level input current	—	—	50	nA
V_{OH}[2]	High-level output voltage	0.8 × VDD[1]	—	—	V
V_{OL}[2]	Low-level output voltage	—	—	0.1 × VDD[1]	V
I_{OH}	High-level source current (VDD[1]= 3.3 V, V_{OH} >= 2.64 V, PAD_DRIVER = 3)	—	40	—	mA
I_{OL}	Low-level sink current (VDD[1]= 3.3 V, V_{OL} = 0.495 V, PAD_DRIVER = 3)	—	28	—	mA
R_{PU}	Internal weak pull-up resistor	—	45	—	kΩ
R_{PD}	Internal weak pull-down resistor	—	45	—	kΩ
V_{IH_nRST}	SiP reset release voltage (CHIP_PU voltage is within the specified range)	0.75 × VDD[1]	—	VDD[1]+ 0.3	V
V_{IL_nRST}	SiP reset voltage (CHIP_PU voltage is within the specified range)	–0.3	—	0.25 × VDD[1]	V

[1] VDD is the I/O voltage for a particular power domain of pins.

[2] V_{OH} and V_{OL} are measured using high-impedance load.

3.5 ADC Characteristics

The measurements in this section are taken with an external 100 nF capacitor connected to the ADC, using DC signals as input, and at an ambient temperature of 25 °C with disabled Wi-Fi.

Table 3-5. ADC Characteristics

Symbol	Min	Max	Unit
DNL (Differential nonlinearity) [1]	–4	4	LSB
INL (Integral nonlinearity)	–8	8	LSB
Sampling rate	—	100	kSPS [2]

[1] To get better DNL results, you can sample multiple times and apply a filter, or calculate the average value.

[2] kSPS means kilo samples-per-second.

Table 3-6. ADC Calibration Results

Parameter	Description	Min	Max	Unit
Total error	ATTEN0, effective measurement range of 0 ~ 850	–5	5	mV
	ATTEN1, effective measurement range of 0 ~ 1100	–6	6	mV
	ATTEN2, effective measurement range of 0 ~ 1600	–10	10	mV
	ATTEN3, effective measurement range of 0 ~ 2900	–50	50	mV

3.6 Current Consumption

3.6.1 RF Current Consumption in Active Mode

The current consumption measurements are taken with a 3.3 V supply at 25 °C of ambient temperature at the RF port. All transmitters' measurements are based on a 100% duty cycle.

Table 3-7. Current Consumption for Wi-Fi (2.4 GHz) in Active Mode

Work Mode	RF Condition	Description	Peak (mA)
Active (RF working)	TX	802.11b, 1 Mbps, DSSS @ 20.0dBm	350
		802.11g, 54 Mbps, OFDM @ 17.0dBm	287
		802.11n, HT20, MCS7 @ 16.5dBm	282
		802.11n, HT40, MCS7 @ 16.5dBm	280
	RX	802.11b/g/n, HT20	100
		802.11n, HT40	105

Note:
The content below is excerpted from *Section Power Consumption in Other Modes* in *ESP32-S3 Series Datasheet*.

3.6.2 Current Consumption in Other Modes

Please note that since the SiP has in-package PSRAM, the current consumption might be higher compared to the measurements below.

Table 3-8. Current Consumption in Modem-sleep Mode

Work mode	Frequency (MHz)	Description	Typ[1] (mA)	Typ[2] (mA)
Modem-sleep[3]	40	WAITI (Dual core in idle state)	13.2	18.8
		Single core running 32-bit data access instructions, the other core in idle state	16.2	21.8
		Dual core running 32-bit data access instructions	18.7	24.4
		Single core running 128-bit data access instructions, the other core in idle state	19.9	25.4
		Dual core running 128-bit data access instructions	23.0	28.8
	80	WAITI	22.0	36.1
		Single core running 32-bit data access instructions, the other core in idle state	28.4	42.6
		Dual core running 32-bit data access instructions	33.1	47.3
		Single core running 128-bit data access instructions, the other core in idle state	35.1	49.6
		Dual core running 128-bit data access instructions	41.8	56.3
	160	WAITI	27.6	42.3
		Single core running 32-bit data access instructions, the other core in idle state	39.9	54.6
		Dual core running 32-bit data access instructions	49.6	64.1
		Single core running 128-bit data access instructions, the other core in idle state	54.4	69.2
		Dual core running 128-bit data access instructions	66.7	81.1
	240	WAITI	32.9	47.6
		Single core running 32-bit data access instructions, the other core in idle state	51.2	65.9
		Dual core running 32-bit data access instructions	66.2	81.3
		Single core running 128-bit data access instructions, the other core in idle state	72.4	87.9
		Dual core running 128-bit data access instructions	91.7	107.9

[1] Current consumption when all peripheral clocks are **disabled**.

[2] Current consumption when all peripheral clocks are **enabled**. In practice, the current consumption might be different depending on which peripherals are enabled.

[3] In Modem-sleep mode, Wi-Fi is clock gated, and the current consumption might be higher when accessing flash. For a flash rated at 80 Mbit/s, in SPI 2-line mode the consumption is 10 mA.

Table 3-9. Current Consumption in Low-Power Modes

Work mode	Description	Typ (μA)
Light-sleep[1]	VDD_SPI and Wi-Fi are powered down, and all GPIOs are high-impedance.	240
Deep-sleep	RTC memory and RTC peripherals are powered up.	8
	RTC memory is powered up. RTC peripherals are powered down.	7

Power off	CHIP_PU is set to low level. The SiP is shut down.	1

[1] In Light-sleep mode, all related SPI pins are pulled up. Please add corresponding PSRAM consumption values, e.g., 140 μA for 8 MB 8-line PSRAM (3.3 V) and 40 μA for 2 MB 4-line PSRAM (3.3 V).

3.7 Reliability

Table 3-10. Reliability Qualifications

Test Item	Test Conditions	Test Standard
ESD (Electro-Static Discharge Sensitivity)	HBM (Human Body Mode)[1] ± 2000 V	JS-001
	CDM (Charge Device Mode)[2] ± 1000 V	JS-002
Latch up	Current trigger ± 200 mA	JESD78
	Voltage trigger 1.5 × VDD_{max}	
Preconditioning	Bake 24 hours @125 °C Moisture soak (level 3: 192 hours @30 °C, 60% RH) IR reflow solder: 260 + 0 °C, 20 seconds, three times	J-STD-020, JESD47, JESD22-A113
TCT (Temperature Cycling Test)	–65 °C / 150 °C, 500 cycles	JESD22-A104
uHAST (Highly Accelerated Stress Test, unbiased)	130 °C, 85% RH, 96 hours	JESD22-A118
HTSL (High Temperature Storage Life)	150 °C, 1000 hours	JESD22-A103
LTSL (Low Temperature Storage Life)	–40 °C, 1000 hours	JESD22-A119

[1] JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

[2] JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

3.8 Wi-Fi Radio

Table 3-11. Wi-Fi RF Characteristics

Name	Description
Center frequency range of operating channel	2412 ~ 2484 MHz
Wi-Fi wireless standard	IEEE 802.11b/g/n

3.8.1 Wi-Fi RF Transmitter (TX) Specifications

Table 3-12. TX Power with Spectral Mask and EVM Meeting 802.11 Standards

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps, DSSS	—	20.0	—
802.11b, 11 Mbps, CCK	—	20.0	—
802.11g, 6 Mbps, OFDM	—	19.0	—
802.11g, 54 Mbps, OFDM	—	17.0	—
802.11n, HT20, MCS0	—	18.5	—
802.11n, HT20, MCS7	—	16.5	—
802.11n, HT40, MCS0	—	18.0	—
802.11n, HT40, MCS7	—	16.5	—

Table 3-13. TX EVM Test[1]

Rate	Min (dB)	Typ (dB)	Limit (dB)
802.11b, 1 Mbps, DSSS	—	–25.0	–10.0
802.11b, 11 Mbps, CCK	—	–25.0	–10.0
802.11g, 6 Mbps, OFDM	—	–23.0	–5.0
802.11g, 54 Mbps, OFDM	—	–30.0	–25.0
802.11n, HT20, MCS0	—	–23.5	–5.0
802.11n, HT20, MCS7	—	–31.5	–27.0
802.11n, HT40, MCS0	—	–25.5	–5.0
802.11n, HT40, MCS7	—	–31.0	–27.0

[1] EVM is measured at the corresponding typical TX power provided in Table 3-12 *Wi-Fi RF Transmitter (TX) Specifications* above.

3.8.2 Wi-Fi RF Receiver (RX) Specifications

Table 3-14. RX Sensitivity

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps, DSSS	—	–97.8	—
802.11b, 2 Mbps, DSSS	—	–95.8	—
802.11b, 5.5 Mbps, CCK	—	–93.6	—
802.11b, 11 Mbps, CCK	—	–88.4	—
802.11g, 6 Mbps, OFDM	—	–93.0	—
802.11g, 9 Mbps, OFDM	—	–91.8	—
802.11g, 12 Mbps, OFDM	—	–90.4	—
802.11g, 18 Mbps, OFDM	—	–88.0	—

Cont'd on next page

Table 3-14 – cont'd from previous page

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11g, 24 Mbps, OFDM	—	–85.0	—
802.11g, 36 Mbps, OFDM	—	–82.0	—
802.11g, 48 Mbps, OFDM	—	–77.6	—
802.11g, 54 Mbps, OFDM	—	–76.0	—
802.11n, HT20, MCS0	—	–92.8	—
802.11n, HT20, MCS1	—	–90.2	—
802.11n, HT20, MCS2	—	–87.6	—
802.11n, HT20, MCS3	—	–84.6	—
802.11n, HT20, MCS4	—	–81.4	—
802.11n, HT20, MCS5	—	–77.0	—
802.11n, HT20, MCS6	—	–75.2	—
802.11n, HT20, MCS7	—	–74.2	—
802.11n, HT40, MCS0	—	–89.4	—
802.11n, HT40, MCS1	—	–87.2	—
802.11n, HT40, MCS2	—	–84.4	—
802.11n, HT40, MCS3	—	–81.4	—
802.11n, HT40, MCS4	—	–78.2	—
802.11n, HT40, MCS5	—	–73.8	—
802.11n, HT40, MCS6	—	–72.4	—
802.11n, HT40, MCS7	—	–71.0	—

Table 3-15. Maximum RX Level

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps, DSSS	—	5	—
802.11b, 11 Mbps, CCK	—	5	—
802.11g, 6 Mbps, OFDM	—	5	—
802.11g, 54 Mbps, OFDM	—	0	—
802.11n, HT20, MCS0	—	5	—
802.11n, HT20, MCS7	—	0	—
802.11n, HT40, MCS0	—	5	—
802.11n, HT40, MCS7	—	0	—

Table 3-16. RX Adjacent Channel Rejection

Rate	Min (dB)	Typ (dB)	Max (dB)
802.11b, 1 Mbps, DSSS	—	35	—
802.11b, 11 Mbps, CCK	—	35	—

Cont'd on next page

Table 3-16 – cont'd from previous page

Rate	Min (dB)	Typ (dB)	Max (dB)
802.11g, 6 Mbps, OFDM	—	31	—
802.11g, 54 Mbps, OFDM	—	14	—
802.11n, HT20, MCS0	—	31	—
802.11n, HT20, MCS7	—	13	—
802.11n, HT40, MCS0	—	19	—
802.11n, HT40, MCS7	—	8	—

3.9 Bluetooth 5 (LE) Radio

Table 3-17. Bluetooth LE RF Characteristics

Name	Description
Center frequency range of operating channel	2402 ~ 2480 MHz
RF transmit power range	–24.0 ~ 20.0 dBm

3.9.1 Bluetooth LE RF Transmitter (TX) Characteristics

Table 3-18. Bluetooth LE - Transmitter Characteristics - 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max. $\lvert f_n \rvert_{n=0,\,1,\,2,\,3,\,\ldots k}$	—	1.7	—	kHz
	Max. $\lvert f_0 - f_n \rvert_{n=2,\,3,\,4,\,\ldots k}$	—	1.6	—	kHz
	Max. $\lvert f_n - f_{n-5} \rvert_{n=6,\,7,\,8,\,\ldots k}$	—	1.1	—	kHz
	$\lvert f_1 - f_0 \rvert$	—	0.4	—	kHz
Modulation characteristics	$\Delta\ F1_{avg}$	—	250.5	—	kHz
	Min. $\Delta\ F2_{max}$ (for at least 99.9% of all $\Delta\ F2_{max}$)	—	198.5	—	kHz
	$\Delta\ F2_{avg}/\Delta\ F1_{avg}$	—	0.85	—	—
In-band emissions	± 2 MHz offset	—	–37	—	dBm
	± 3 MHz offset	—	–42	—	dBm
	> ± 3 MHz offset	—	–44	—	dBm

Table 3-19. Bluetooth LE - Transmitter Characteristics - 2 Mbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max. $\lvert f_n \rvert_{n=0,\,1,\,2,\,3,\,\ldots k}$	—	2.5	—	kHz
	Max. $\lvert f_0 - f_n \rvert_{n=2,\,3,\,4,\,\ldots k}$	—	1.3	—	kHz
	Max. $\lvert f_n - f_{n-5} \rvert_{n=6,\,7,\,8,\,\ldots k}$	—	1.0	—	kHz
	$\lvert f_1 - f_0 \rvert$	—	0.4	—	kHz
Modulation characteristics	$\Delta\ F1_{avg}$	—	498.0	—	kHz

Cont'd on next page

Table 3-19 – cont'd from previous page

Parameter	Description	Min	Typ	Max	Unit
	Min. $\Delta F2_{max}$ (for at least 99.9% of all $\Delta F2_{max}$)	—	429.0	—	kHz
	$\Delta F2_{avg}/\Delta F1_{avg}$	—	0.91	—	—
In-band emissions	± 4 MHz offset	—	–42	—	dBm
	± 5 MHz offset	—	–44	—	dBm
	> ± 5 MHz offset	—	–47	—	dBm

Table 3-20. Bluetooth LE - Transmitter Characteristics - 125 Kbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max. $\lvert f_n \rvert_{n=0,\,1,\,2,\,3,\,\ldots k}$	—	0.5	—	kHz
	Max. $\lvert f_0 - f_n \rvert_{n=1,\,2,\,3,\,\ldots k}$	—	0.2	—	kHz
	$\lvert f_0 - f_3 \rvert$	—	0.2	—	kHz
	Max. $\lvert f_n - f_{n-3} \rvert_{n=7,\,8,\,9,\,\ldots k}$	—	0.7	—	kHz
Modulation characteristics	$\Delta F1_{avg}$	—	250.4	—	kHz
	Min. $\Delta F1_{max}$ (for at least 99.9% of all $\Delta F1_{max}$)	—	240.8	—	kHz
In-band emissions	± 2 MHz offset	—	–37	—	dBm
	± 3 MHz offset	—	–42	—	dBm
	> ± 3 MHz offset	—	–44	—	dBm

Table 3-21. Bluetooth LE - Transmitter Characteristics - 500 Kbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max. $\lvert f_n \rvert_{n=0,\,1,\,2,\,3,\,\ldots k}$	—	0.5	—	kHz
	Max. $\lvert f_0 - f_n \rvert_{n=1,\,2,\,3,\,\ldots k}$	—	0.5	—	kHz
	$\lvert f_0 - f_3 \rvert$	—	0.2	—	kHz
	Max. $\lvert f_n - f_{n-3} \rvert_{n=7,\,8,\,9,\,\ldots k}$	—	0.7	—	kHz
Modulation characteristics	$\Delta F2_{avg}$	—	211.5	—	kHz
	Min. $\Delta F2_{max}$ (for at least 99.9% of all $\Delta F2_{max}$)	—	198.1	—	kHz
In-band emissions	± 2 MHz offset	—	–37	—	dBm
	± 3 MHz offset	—	–42	—	dBm
	> ± 3 MHz offset	—	–44	—	dBm

3.9.2 Bluetooth LE RF Receiver (RX) Characteristics

Table 3-22. Bluetooth LE - Receiver Characteristics - 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	–96.0	—	dBm
Maximum received signal @30.8% PER	—	—	8	—	dBm

Cont'd on next page

Table 3-22 – cont'd from previous page

Parameter		Description	Min	Typ	Max	Unit
C/I and receiver selectivity performance	Co-channel	F = F0 MHz	—	8	—	dB
	Adjacent channel	F = F0 + 1 MHz	—	4	—	dB
		F = F0 – 1 MHz	—	4	—	dB
		F = F0 + 2 MHz	—	–23	—	dB
		F = F0 – 2 MHz	—	–23	—	dB
		F = F0 + 3 MHz	—	–34	—	dB
		F = F0 – 3 MHz	—	–34	—	dB
		F ≥ F0 + 4 MHz	—	–36	—	dB
		F ≤ F0 – 4 MHz	—	–37	—	dB
	Image frequency	—	—	–36	—	dB
	Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–39	—	dB
		F = F_{image} – 1 MHz	—	–34	—	dB
Out-of-band blocking performance		30 MHz ~ 2000 MHz	—	–12	—	dBm
		2003 MHz ~ 2399 MHz	—	–18	—	dBm
		2484 MHz ~ 2997 MHz	—	–16	—	dBm
		3000 MHz ~ 12.75 GHz	—	–10	—	dBm
Intermodulation		—	—	–29	—	dBm

Table 3-23. Bluetooth LE - Receiver Characteristics - 2 Mbps

Parameter		Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER		—	—	–91.5	—	dBm
Maximum received signal @30.8% PER		—	—	3	—	dBm
C/I and receiver selectivity performance	Co-channel	F = F0 MHz	—	8	—	dB
	Adjacent channel	F = F0 + 2 MHz	—	4	—	dB
		F = F0 – 2 MHz	—	4	—	dB
		F = F0 + 4 MHz	—	–27	—	dB
		F = F0 – 4 MHz	—	–27	—	dB
		F = F0 + 6 MHz	—	–38	—	dB
		F = F0 – 6 MHz	—	–38	—	dB
		F ≥ F0 + 8 MHz	—	–41	—	dB
		F ≤ F0 – 8 MHz	—	–41	—	dB
	Image frequency	—	—	–27	—	dB
	Adjacent channel to image frequency	F = F_{image} + 2 MHz	—	–38	—	dB
		F = F_{image} – 2 MHz	—	4	—	dB
Out-of-band blocking performance		30 MHz ~ 2000 MHz	—	–15	—	dBm
		2003 MHz ~ 2399 MHz	—	–21	—	dBm
		2484 MHz ~ 2997 MHz	—	–21	—	dBm
		3000 MHz ~ 12.75 GHz	—	–9	—	dBm
Intermodulation		—	—	–29	—	dBm

Table 3-24. Bluetooth LE - Receiver Characteristics - 125 Kbps

Parameter		Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER		—	—	–102.5	—	dBm
Maximum received signal @30.8% PER		—	—	8	—	dBm
C/I and receiver selectivity performance	Co-channel	F = F0 MHz	—	4	—	dB
	Adjacent channel	F = F0 + 1 MHz	—	1	—	dB
		F = F0 – 1 MHz	—	2	—	dB
		F = F0 + 2 MHz	—	–26	—	dB
		F = F0 – 2 MHz	—	–26	—	dB
		F = F0 + 3 MHz	—	–36	—	dB
		F = F0 – 3 MHz	—	–39	—	dB
		F ≥ F0 + 4 MHz	—	–42	—	dB
		F ≤ F0 – 4 MHz	—	–43	—	dB
	Image frequency	—	—	–42	—	dB
	Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–43	—	dB
		F = F_{image} – 1 MHz	—	–36	—	dB

Table 3-25. Bluetooth LE - Receiver Characteristics - 500 Kbps

Parameter		Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER		—	—	–99.0	—	dBm
Maximum received signal @30.8% PER		—	—	8	—	dBm
C/I and receiver selectivity performance	Co-channel	F = F0 MHz	—	4	—	dB
	Adjacent channel	F = F0 + 1 MHz	—	1	—	dB
		F = F0 – 1 MHz	—	0	—	dB
		F = F0 + 2 MHz	—	–24	—	dB
		F = F0 – 2 MHz	—	–24	—	dB
		F = F0 + 3 MHz	—	–37	—	dB
		F = F0 – 3 MHz	—	–39	—	dB
		F ≥ F0 + 4 MHz	—	–38	—	dB
		F ≤ F0 – 4 MHz	—	–42	—	dB
	Image frequency	—	—	–38	—	dB
	Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–42	—	dB
		F = F_{image} – 1 MHz	—	–37	—	dB

4 Schematics

This is the reference designs of ESP32-S3-PICO-1.

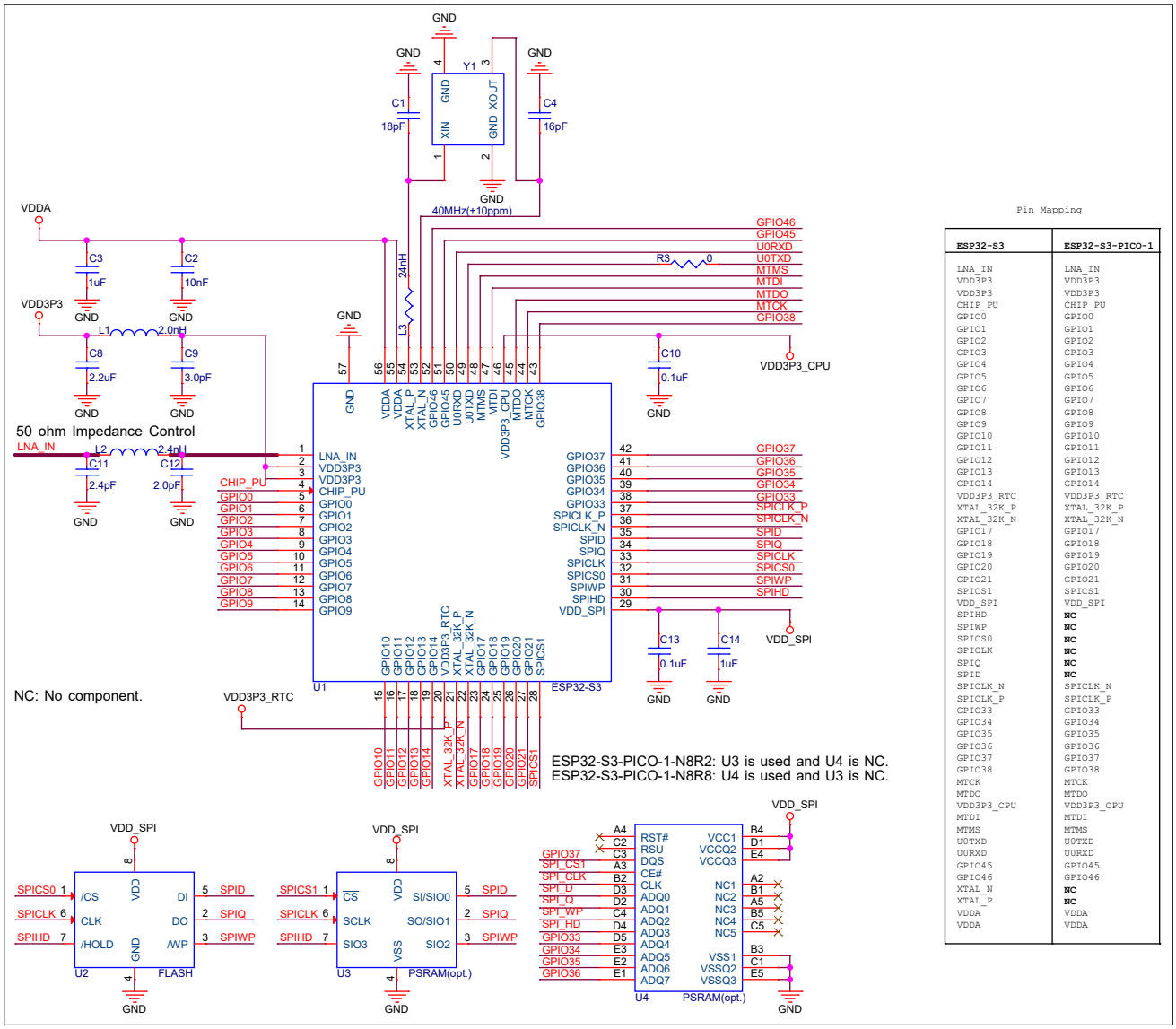


Figure 4-1. ESP32-S3-PICO-1 Schematics

5 Peripheral Schematics

This is the typical application circuit of ESP32-S3-PICO-1 connected with peripheral components (for example, power supply, antenna, reset button, JTAG interface, and UART interface).

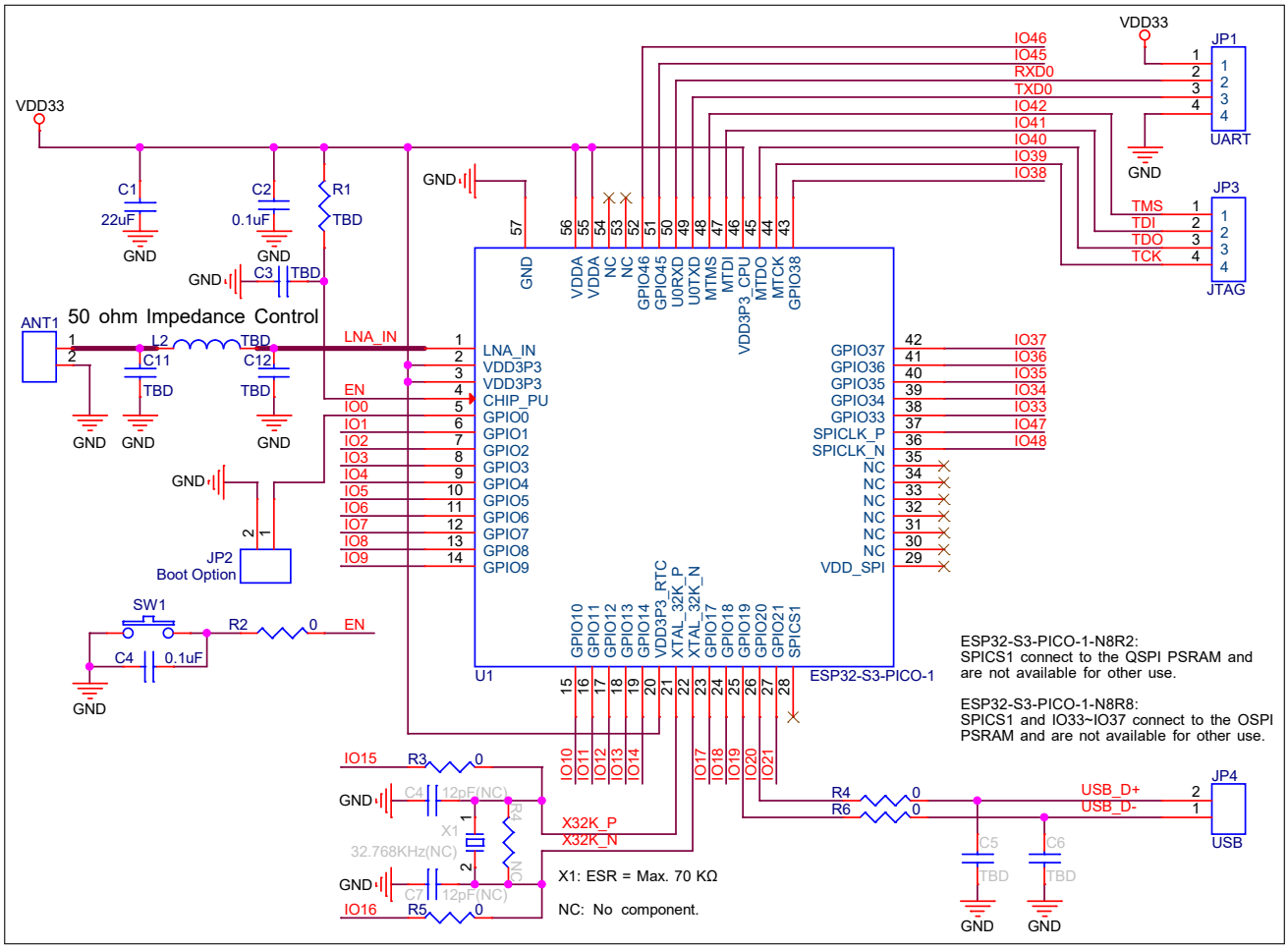
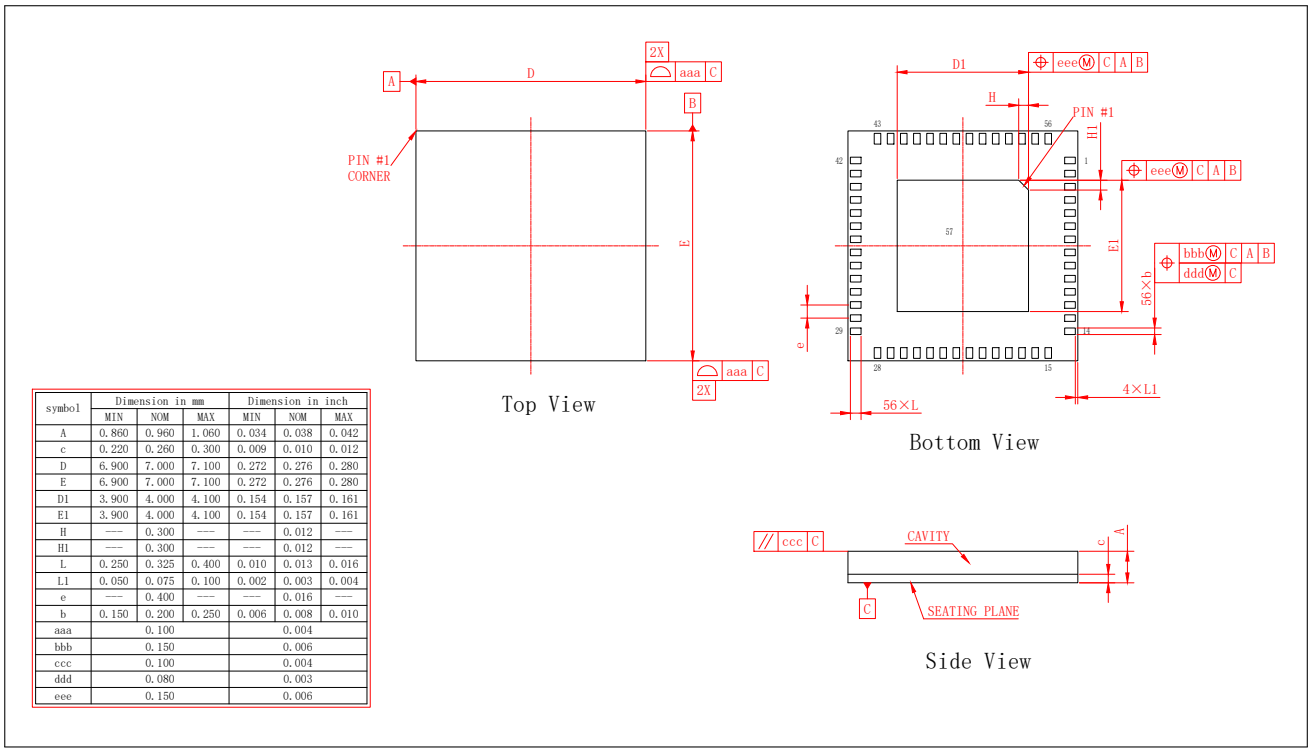


Figure 5-1. ESP32-S3-PICO-1 Peripheral Schematics

To ensure that the power supply to ESP32-S3-PICO-1 is stable during power-up, it is advised to add an RC delay circuit at the CHIP_PU pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 1 μF. However, specific parameters should be adjusted based on the power-up timing of the SiP and the power-up and reset sequence timing of the chip. For ESP32-S3's power-up and reset sequence timing diagram, please refer to *ESP32-S3 Series Datasheet* > Section *Power Supply*.

6 Packaging



symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.860	0.960	1.060	0.034	0.038	0.042
c	0.220	0.260	0.300	0.009	0.010	0.012
D	6.900	7.000	7.100	0.272	0.276	0.280
E	6.900	7.000	7.100	0.272	0.276	0.280
D1	3.900	4.000	4.100	0.154	0.157	0.161
E1	3.900	4.000	4.100	0.154	0.157	0.161
H	---	0.300	---	---	0.012	---
H1	---	0.300	---	---	0.012	---
L	0.250	0.325	0.400	0.010	0.013	0.016
L1	0.050	0.075	0.100	0.002	0.003	0.004
e	---	0.400	---	---	0.016	---
b	0.150	0.200	0.250	0.006	0.008	0.010
aaa	0.100			0.004		
bbb	0.150			0.006		
ccc	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		

Figure 6-1. LGA56 (7x7 mm) Package

Note:

- The pins of the ESP32-S3-PICO-1 series are numbered in an anti-clockwise direction from Pin 1 in the top view.
- For information about tape, reel, and product marking, please refer to *Espressif Chip Packaging Information*.

7 Product Handling

7.1 Storage Conditions

The products sealed in moisture barrier bags (MBB) should be stored in a non-condensing atmospheric environment of < 40 °C and /90%RH. The SiP is rated at the moisture sensitivity level (MSL) of 3.

After unpacking, the SiP must be soldered within 168 hours with the factory conditions 25±5 °C and /60%RH. If the above conditions are not met, the SiP needs to be baked.

7.2 Reflow Profile

Solder the SiP in a single reflow.

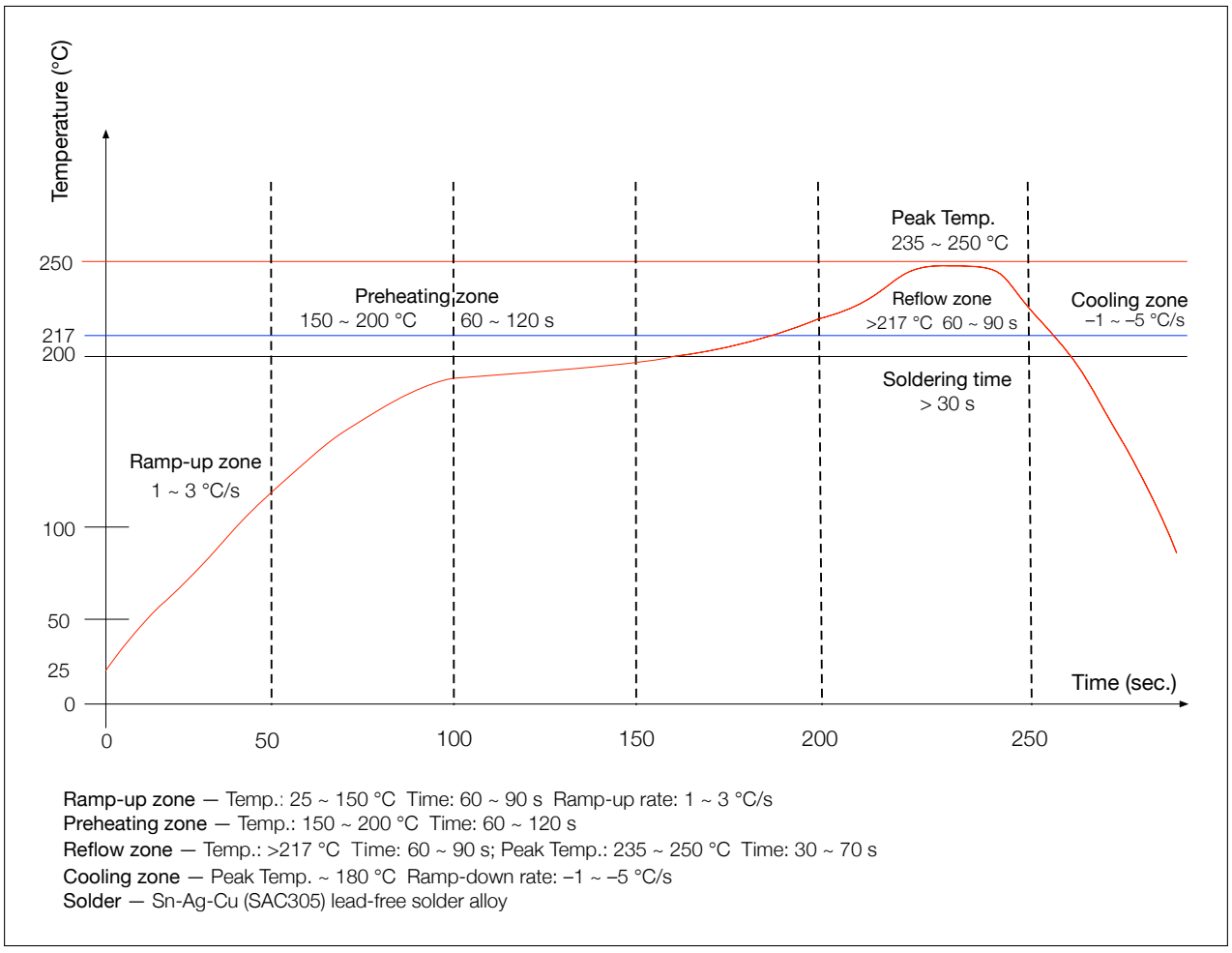


Figure 7-1. Reflow Profile

7.3 Ultrasonic Vibration

Avoid exposing Espressif SiPs to vibration from ultrasonic equipment, such as ultrasonic welders or ultrasonic cleaners. This vibration may induce resonance in the in-SiP crystal and lead to its malfunction or even failure. As a consequence, **the SiP may stop working or its performance may deteriorate**.

8 Related Documentation and Resources

Related Documentation

- ESP32-S3 Series Datasheet – Specifications of the ESP32-S3 hardware.
- ESP32-S3 Technical Reference Manual – Detailed information on how to use the ESP32-S3 memory and peripherals.
- ESP32-S3 Hardware Design Guidelines – Guidelines on how to integrate the ESP32-S3 into your hardware product.
- ESP32-S3 Series SoC Errata – Descriptions of known errors in ESP32-S3 series of SoCs.
- *Certificates*
  https://espressif.com/en/support/documents/certificates
- *ESP32-S3 Product/Process Change Notifications (PCN)*
  https://espressif.com/en/support/documents/pcns?keys=ESP32-S3
- *ESP32-S3 Advisories* – Information on security, bugs, compatibility, component reliability.
  https://espressif.com/en/support/documents/advisories?keys=ESP32-S3
- *Documentation Updates and Update Notification Subscription*
  https://espressif.com/en/support/download/documents

Developer Zone

- ESP-IDF Programming Guide for ESP32-S3 – Extensive documentation for the ESP-IDF development framework.
- *ESP-IDF* and other development frameworks on GitHub.
  https://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
  https://espressif.com/en/support/download/sdks-demos

Products

- *ESP32-S3 Series SoCs* – Browse through all ESP32-S3 SoCs.
  https://espressif.com/en/products/socs?id=ESP32-S3
- *ESP32-S3 Series Modules* – Browse through all ESP32-S3-based modules.
  https://espressif.com/en/products/modules?id=ESP32-S3
- *ESP32-S3 Series DevKits* – Browse through all ESP32-S3-based devkits.
  https://espressif.com/en/products/devkits?id=ESP32-S3
- *ESP Product Selector* – Find an Espressif hardware product suitable for your needs by comparing or applying filters.
  https://products.espressif.com/#/product-selector?language=en

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  https://espressif.com/en/contact-us/sales-questions

Revision History

Date	Version	Release notes
2023-07-21	v1.0	Added the following sections: • Section 3.4 *DC Characteristics (3.3 V, 25 °C)* • Section 3.5 *ADC Characteristics* • Section 3.6 *Current Consumption* • Section 3.7 *Reliability* • Section 3.8 *Wi-Fi Radio* • Section 3.9 *Bluetooth 5 (LE) Radio* Updated the following section: • Updated Section 2.3 *Strapping Pins* • Updated Section 4 *Schematics* • Updated Section 5 *Peripheral Schematics* Other minor updates
2023-03-30	v0.2	Updated Figure *Peripheral Schematics*
2022-09-23	v0.1	Preliminary

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